IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Masaya MURANAKA et al.

Appln. No.:

Filed: HEREWITH

For: METHOD OF DECIDING ERROR RATE AND SEMICONDUCTOR
INTEGRATED CIRCUIT DEVICE

* * *

<u>INFORMATION DISCLOSURE STATEMENT</u>

Commissioner for Patents
P.O. Box 1450
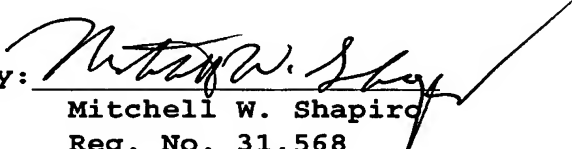Alexandria, VA   22313-1450

Sir:

Applicants wish to make of record the documents cited

in prior Application No. 09/875,961 filed June 8, 2001,

whether cited by Applicants or by the Patent Office.   The

documents are listed on the attached Form PTO-1449.

Respectfully submitted,

MWS:adc

Miles & Stockbridge P.C.   By: _____
1751 Pinnacle Drive   Mitchell W. Shapiro
Suite 500   Reg. No. 31,568
McLean, Virginia   22102-3833
(703) 903-9000

March 25, 2004

FORM PTO-1449	Atty. Docket No.	Appln. No.
	XA-9485A	
LIST OF DOCUMENTS CITED BY APPLICANT		
	Applicant	
	Masaya MURANAKA et al.	
	Filing Date	Group
	HEREWITH	

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
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	AB	6,065,146 A	05/2000	Bosshart, Patrick	714	754	
	AC	6,236,602 B1	05/2001	Patti, Robert	365	201	
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	AF						
	AG						
	AH						
	AI						

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	AK	07-262794	10/13/95	Japan			Abstract
	AL	11-007760 A	01/12/99	Japan			Abstract
	AM						
	AN						
	AO						

OTHER (including author, title, date, pertinent pages, etc.)

	AP	Mano, T.; Yamada, J.; Inoue, J.; Nakajima, S.; Circuit Techniques For A VLSI Memory, IEEE Journal of Solid-State Circuits, Volume: 18 Issue: 5, October 1983, Pages 463-470
	AQ	
	AR	

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.